Remarks

Claim 3 was previously cancelled. Claims 1, 2, 5, 7-9, 11, 12, 14, 15, 17 and 20-23 are presently amended. Claims 1, 2 and 4-23 are pending in this application. The Examiner has rejected claims 1, 2 and 4-23 under 35 U.S.C. § 102(e) as being unpatentable over U.S. Patent No. 7,017,054 to Schuckle, et al. Applicant respectfully traverses the Examiner's rejections.

A. Remarks Regarding Telephone Interview With Examiner

On December 23, 2008, Applicant's representative participated in a telephone interview with the Examiner. Thereafter, on January 6, 2009, an Interview Summary was mailed to Applicant. Applicant does not dispute the Summary. Discussed in the interview were the "wherein" clauses of claim 1, and it was agreed that claim amendments would be submitted in light of that discussion.

B. Remarks Regarding Rejection of Claims 1, 2 and 4-23 Under 35 U.S.C. § 102(e)

The Examiner has rejected independent claims 1, 5, 12 17 and 21 as being anticipated by Schuckle. Applicant respectfully submits that the cited reference does not anticipate the claims. Schuckle standing alone does not contain each and every element of the claimed invention and, as such, the reference cannot anticipate the amended claims. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." M.P.E.P. § 2131 (citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987)); Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989) ("The identical invention must be shown in as complete detail as is contained in the . . . claim.").

In particular, Schuckle fails to disclose "a write tracking buffer external to the processor, wherein the write tracking buffer is communicatively coupled to the cache via the processor and to the system memory. . . wherein the memory controller hub is operable to: initialize the write tracking buffer when the processor enters a low power state; identify one or more writes to the system memory made during the period that the processor is in the low power state; determine if the write tracking buffer is full during the period that the processor is in the low power state; and if the write tracking buffer is not full, record the addresses of the one or more writes; and wherein the processor is operable to write to the system memory one or more lines of cache prior to the processor entering its low power state," as required by amended claim 1 and as similarly required by amended 5, 12, 17 and 21.

The amendments directed to the above limitations are supported by the specification of the present application. For example, the specification discloses a write tracking buffer external to the processor and communicatively coupled to the cache via the processor and to the system memory. (*See, e.g.*, Spec. at Fig. 1; *id.* at p. 6 ln. 22 to p. 7 ln. 2.) A memory controller hub initializes the write tracking buffer when the processor enters a low power state. (*See, e.g., id.* at p. 7 lns. 11-13.) The memory controller hub identifies writes to system memory while the processor is in a low power state. (*See, e.g., id.* at Fig. 2; *id.* at p. 7 lns. 14-26.) The memory controller hub determines if the write tracking buffer is full during the low power state period. (*See, e.g., id.*) If the write tracking buffer is not full, the memory controller hub records addresses of the writes. (*See, e.g., id.*) The processor writes to system memory lines of cache prior to the processor entering its low power state. (*See, e.g., id.* at p. 7 lns. 3-13.) Applicant cannot find, nor does the Examiner cite, in Schuckle any discussion of these claim limitations.

Schuckle discusses an index list stored inside the processor's RAM which resides *inside* the processor. (*See* Schuckle 7:1-18.) "The requirement is that when the cache resides *inside* the processor (this is standard practice in many processors), then the processor must be in a power state that supports 'snooping' of memory accesses when they occur." (Schuckle 7:9-12 (emphasis added).) The index list is drawn to "the addresses of memory locations that are stored in the processor's cache RAM." (*See* Schuckle 7:1-3.) Thus, Schuckle's index list is not equivalent to a write tracking buffer *external* to the processor and communicatively coupled to the cache via the processor and to the system memory, as is required by the claims.

Moreover, Schuckle's low power state ("non-cacheable state") specifically requires that the processor's caches be "unable to perform [and] typically ignore any snoops." (*See* Schuckle 7:1-18.) When Schuckle's processor is in a low power state, the hardware and/or software must "wake" the processor when the first data access request is detected. (*See* Schuckle 7:4-18.) No data access requests are processed during Schuckle's low power period. Data access requests are merely detected during Schuckle's low power period. This is not the same as a memory controller hub that—without "waking" the processor—records writes to a write tracking buffer while the processor is in a low power state. Hence, Schuckle does not disclose a memory controller hub that: (1) tracks writes to system memory; (2) records writes to a write tracking buffer; and (3) checks if the write tracking buffer is full—all during the period when the processor is in a low power state and without "waking" the processor.

Furthermore, Schuckle brief mention of an index list fails to disclose initializing a write tracking buffer upon the processor's entering the low power state. There is no mention of a buffer being initialized for use during the Schuckle's low power ("non-cacheable") period. Additionally, Schuckle simply provides no discussion of the processor writing to system memory

lines of cache prior to the processor entering its low power state. Therefore, for at least these reasons, Schuckle fails to disclose the claims limitations.

As Schuckle fails to teach or disclose each and every element of independent claims 1, 5, 12 17 and 21, Schuckle does not anticipate these claims. Applicant respectfully submits that these independent claims are allowable. Additionally, Applicant submits that dependent claims 2, 4, 6-11, 13-16, 18-20, 22 and 23 are allowable, as they depend from otherwise allowable base claims.

C. Remarks Regarding Rejection of Dependent Claims 2-7, 9-14 and 16-20 Under 35 U.S.C. § 102

The rejection of dependent claims 2, 4, 6-11, 13-16, 18-20, 22 and 23 will not be discussed individually herein, as each of these claims depends, either directly or indirectly, from an otherwise allowable base claim.

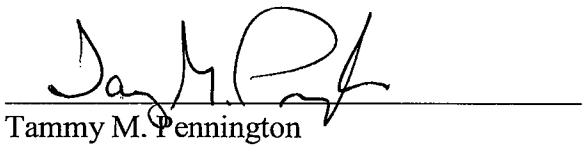
D. No Waiver

All of Applicant's arguments and amendments are without prejudice or disclaimer. Additionally, Applicant has merely discussed example distinctions from the cited references. Other distinctions may exist, and Applicant reserves the right to discuss these additional distinctions in a later Response or on Appeal, if appropriate. By not responding to additional statements made by examiner, Applicant does not acquiesce to examiner's additional statements, such as, for example, any statements relating to what would be obvious to a person of ordinary skill in the art. The example distinctions discussed by Applicant are sufficient to overcome the anticipation rejections. The current amendments to the claims are sufficient to overcome the novelty and obviousness rejections.

Conclusion

Applicant respectfully submits that the pending claims 1, 2 and 4-23 of the present invention, as amended, are allowable. Applicant respectfully requests that the rejection of the pending claims be withdrawn and that these claims be passed to issuance.

Respectfully submitted,



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Date: January 15, 2009